REMARKS

The Examiner has rejected Claim 9 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has clarified what is being claimed to overcome this rejection.

The Examiner has further rejected Claims 1-8, 10-18, 20-29 and 31-34 under 35 U.S.C. 102(b) as being anticipated by Baldwin, U.S. Patent 5,764,228. The Examiner has also rejected Claims 19 and 30 under 35 U.S.C. 103(a) as being unpatentable over Baldwin, U.S. Patent 5,764,228, in view of Chan et al., U.S. Patent 6,163,837. Applicant respectfully disagrees with such rejections, especially in view of the amendments made hereinabove.

In particular, the Examiner has relied on various passages in Baldwin to show applicant's specific claimed instructions in the prior art. Applicant emphasizes that such passages are taken out of the context of applicant's claimed instructions.

For example, the Examiner relies on the following excerpt from Baldwin to show applicant's claimed "move instruction."

> "StartXDom
> Initial X value for the dominant edge in trapezoid filling, or initial X value in line drawing.
> dXDom Value added when moving from one scanline (or sub scanline) to the next for the dominant edge in trapezoid filling.
> Also holds the change in X when plotting lines so for Y major lines this will be some fraction (dx/dy), otherwise it is normally .+-. 1.0, depending on the required scanning direction.
> StartXSub
> Initial X value for the subordinate edge.
> dXSub Value added when moving from one scanline (or sub scanline) to the next for the subordinate edge in trapezoid filling.
> StartY Initial scanline (or sub scanline) in trapezoid filling, or initial Y position for line drawing.
> dY Value added to Y to move from one scanline to the next.
> For X major lines this will be some fraction (dy/dx), otherwise it is normally .+-. 1.0, depending on the required scanning direction." (col. 43, lines 40-55)

Such excerpt, however, merely suggests a plurality of "control registers," where one of such registers is used to move from one scanline to the next. This clearly fails to meet a "move instruction" in a "programmable ... instruction set," as claimed.

Further, the Examiner relies on the following excerpts from Baldwin to show applicant's claimed "multiply instruction."

> "Again, it should be noted that all operations above the block marked "Rasterization" would be performed by a host processor, or possibly by a "geometry engine" (i.e. a dedicated processor which performs rapid matrix multiplies and related data manipulations), but would normally not be performed by a dedicated rendering processor such as that of the presently preferred embodiment." (col. 4, lines 50-55)

> "The width is specified as the sum of selected partial products so a full multiply operation is not needed." (col. 30, lines 1-2)

Still yet, the Examiner relies on the following excerpt from Baldwin to show applicant's claimed "add instruction," and "multiply and add instruction."

> "The width is specified as the sum of selected partial products so a full multiply operation is not needed." (col. 30, lines 1-2)

The foregoing excerpts, however, merely make independent suggestions of the concepts of adding and multiplying in separate contexts. It is important to note that, in Baldwin, there is simply no single instruction that is designated as a "multiply and add instruction" which combines adding and multiplying operations in the specific context of a "programmable ... instruction set," as claimed by applicant. Only applicant teaches and claims such a combination of functionality in a single instruction as part of a "programmable ... instruction set."

Even still, the Examiner relies on the following excerpt from Baldwin to show applicant's claimed "minimum instruction" and "maximum instruction."

> "GUI systems (such as Windows, Windows NT and X) usually have the origin of the coordinate system at the top left corner of the screen but this is not true for all graphics systems. For instance OpenGL uses the bottom left corner as its origin. The WindowOrigin bit in the LBReadMode register selects the top left (0) or bottom left (1) as the origin." (col. 27, line 65 through col. 28, line 5)

Such excerpt, however, fails to disclose, teach or suggest any sort of "minimum instruction" and "maximum instruction," in the specific context of a "programmable ... instruction set," as claimed.

The Examiner continues by relying on the following excerpt from Baldwin to show applicant's claimed "exponential base two (2) instruction" and "logarithm base two (2) instruction."

> "These address calculations translate a 2D address into a linear address, so non power of two framebuffer widths (i.e. 1280) are economical in memory." (col. 29, lines 65-67)

Such excerpt, however, merely suggests non power of two framebuffer widths. However, it fails to disclose, teach or suggest any sort of "exponential base two (2) instruction" and "logarithm base two (2) instruction," in the specific context of a "programmable ... instruction set," as claimed.

Still yet, the Examiner has failed to show applicant's claimed "reciprocal instruction."

It appears that the Examiner has merely gleaned similar words in Baldwin in an effort to show applicant's specifically claimed instruction set in the prior art. Applicant contends that such gleaning is improper, particularly because the foregoing passages in Baldwin do not relate to specific "instructions" that are components of a predetermined "instruction set" that may be used to take advantage of advanced features in a graphics hardware environment. Simply nowhere in the prior art is there disclosed, taught or suggested any sort of "instructions [that] include a no operation instruction, move instruction, multiply instruction, addition instruction, multiply and addition instruction, reciprocal instruction, reciprocal square root instruction, three component dot product instruction, four component dot product instruction, minimum instruction, maximum instruction, fraction instruction, exponential base two (2) instruction, and logarithm base two (2) instruction," as claimed for enhanced "pixel data processing."

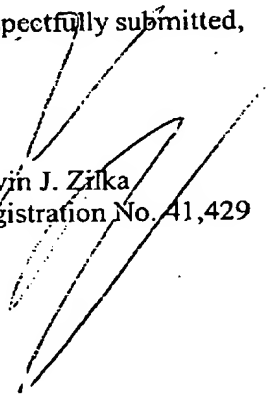
It appears that the Examiner has not considered Claims 31-34 entered by preliminary amendment on December 11, 2001. Such claims have been re-entered with the above limitations, and are considered allowable for the reasons set forth above.

Still yet, applicant contends that the Examiner's previous action is deficient in various other respects. For example, the Examiner relies on col. 40, lines 40-52 and col. 52, lines 36-67 to show in the prior art applicant's claimed "swizzling the pixel data prior to performing the programmable operations thereon." Applicant respectfully disagrees with such interpretation, especially now that the "swizzling" is claimed to "include a component re-mapping."

All of the independent claims are thus deemed allowable along with any claims depending therefrom. An allowance or a specific prior art showing of applicant's claimed features is respectfully requested.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP036).

Respectfully submitted,



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